DATA SHEET
( DOC No. HM01B0-DS )

HM01B0
1/11" 320 x 320 • QVGA 60FPS
CMOS Image Sensor
Preliminary version 05 September, 2016
HM01B0 Ultra Low Power
1/11” 320 x 320 • QVGA 60FPS CMOS Image Sensor

Features
- Ultra Low Power Image Sensor designed for Always-on vision devices and applications
- High sensitivity 3.6µ BrightSense™ pixel technology
- 324 x 324 active pixel resolution with support for QVGA window, vertical flip and horizontal mirror readout
- <1.1mW QVGA resolution at 30FPS, < 2mW QVGA resolution at 30FPS
- Programmable black level calibration target, frame size, frame rate, exposure, analog gain (up to 8x) and digital gain (up to 4x)

Key Parameters

<table>
<thead>
<tr>
<th>Sensor parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Array (Active/ Effective)</td>
<td>324 x 324 / 320 x 320</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>3.6µm x 3.6µm</td>
</tr>
<tr>
<td>Image Diagonal</td>
<td>1.63mm</td>
</tr>
<tr>
<td>Optical Format</td>
<td>Full frame 1/11&quot;; QVGA 1/13&quot;</td>
</tr>
<tr>
<td>Color Filter Array</td>
<td>Bayer, Monochrome</td>
</tr>
<tr>
<td>Shutter Type</td>
<td>Electronic Rolling Shutter</td>
</tr>
<tr>
<td>Frame Rate (Max.)</td>
<td>8-bit, 320p 45FPS @ 6MHz</td>
</tr>
<tr>
<td>(8-bit interface)</td>
<td>8-bit, QVGA 60FPS @ 6MHz</td>
</tr>
<tr>
<td>Frame Rate Max (4-bit interface)</td>
<td>8-bit, 320p 45FPS @ 12MHz</td>
</tr>
<tr>
<td>Frame Rate Max (1-bit interface)</td>
<td>8-bit, QVGA 45FPS @ 36MHz</td>
</tr>
<tr>
<td>Supply Voltage (Typ.)</td>
<td>AVDD 2.8V</td>
</tr>
<tr>
<td>Digital Output</td>
<td>Motion Interrupt (Active High)</td>
</tr>
<tr>
<td>Power Consumption (Typ.)</td>
<td>8-bit, QQVGA 30FPS 1.1mW</td>
</tr>
<tr>
<td>Temperature</td>
<td>Operating -30 °C to 85 °C</td>
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Order Information

<table>
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<tr>
<th>Part no.</th>
<th>Color option</th>
<th>Operating / Storage temperature</th>
<th>Package</th>
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<tbody>
<tr>
<td>HM01B0-AWA</td>
<td>RGB</td>
<td>- 20 °C to 85 °C / -30 °C to 85 °C</td>
<td>CSP</td>
</tr>
<tr>
<td>HM01B0-MWA</td>
<td>Mono</td>
<td>- 20 °C to 85 °C / -30 °C to 85 °C</td>
<td>CSP</td>
</tr>
<tr>
<td>HM01B0-AGA</td>
<td>RGB</td>
<td>- 20 °C to 85 °C / -30 °C to 85 °C</td>
<td>Bare Die</td>
</tr>
<tr>
<td>HM01B0-MGA</td>
<td>Mono</td>
<td>- 20 °C to 85 °C / -30 °C to 85 °C</td>
<td>Bare Die</td>
</tr>
<tr>
<td>HM01B0-ANA</td>
<td>RGB</td>
<td>- 20 °C to 85 °C / -30 °C to 85 °C</td>
<td>NeoPAC</td>
</tr>
<tr>
<td>HM01B0-MNA</td>
<td>Mono</td>
<td>- 20 °C to 85 °C / -30 °C to 85 °C</td>
<td>NeoPAC</td>
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### Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description of changes</th>
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<tbody>
<tr>
<td>01</td>
<td>2016/02/04</td>
<td>New setup.</td>
</tr>
</tbody>
</table>
| 02      | 2016/04/26 | 1. Add test pattern for QQVGA mode.  
2. Modify QVGA window readout and full frame size.  
3. Modify clock divider.  
4. Remove hardware trigger N frame output mode.  
5. Modify IOVDD voltage to 1.8V /2.8V.  
6. Correct AGAIN setting.  
7. Constraint for line length and frame length.  
8. The minimum integration time is 2 rows.  
9. Modify PCLKO polarity in gate mode.  
10. Correct wrong pin name HSYNC and VSYNC in IO control options.  
11. Modify maximum frame rate from 51 FPS to 45 FPS for full frame.  
12. Add description: QQVGA do not support the Bayer sensor version.  
13. Modify stop mode to standby mode in rest.  
| 03      | 2016/05/13 | 1. Modify the description in Monochrome QQVGA using Pixel Binning and Features  
2. Rename 5.2.1, 5.2.2,5.3.1 and 5.3.2  
3. Add output pin status control by register and remove IO status in table 4.  
4. Remove register of GROI and RGB stat ratio.  
5. Add sensor address control register.  
6. Modify clock divider.  
7. Add VSYNC, HSYNC shift register.  
8. Modify power consumption QQVGA 30FPS from 670 µW to 1.1mW. |
| 04      | 2016/08/22 | Page 2  
1. Modify ‘Key Parameters’.
Page 15  
2. Modify ‘Figure 4.1: ISP blocks’.  
Page 23–24  
3. Modify chapter ‘6.1 Operating modes’.  
Page 24  
Page 26  
5. Modify chapter ‘6.4 Clock setup’.  
6. Modify chapter ‘6.4.1 MCLK and self-oscillator mode switch’.  
Page 27  
7. Modify ‘Figure 6.5: Non-gated and gated serial data clock option’.  
Page 29  
8. Modify ‘Figure 6.7: 6-bit and 8-bit RAW output format on 4-bit data IO interface.  
9. Modify ‘Figure 6.8: RAW output format on serial data IO interface’.  
Page 30  
10. Add chapter ‘7.1 I2C slave address ID’.  
Page 32  
11. Modify chapter ‘8.1 Frame retiming’.  
12. Remove Modify ‘Table 8.1: Global analog gain settings’.  
13. Add chapter ‘8.3 Suggestion for analog gain and digital gain’.  
Page 38  

## Revision History

<table>
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<td>Page 40</td>
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<tr>
<td></td>
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<td>15. Modify chapter ‘10.2 Operating voltages’.</td>
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<td>16. Modify chapter ‘10.3 DC characteristics’.</td>
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<td>17. Modify chapter ‘10.4 Master clock input (MCLK)’.</td>
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<td>18. Modify chapter ‘10.6 Parallel interface timing characteristics’.</td>
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<td>19. Modify chapter ‘10.7 Serial interface timing characteristics’.</td>
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<td>05</td>
<td>2016/09/13</td>
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<td>1. Modify ‘Order Information’.</td>
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<td></td>
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<td>2. Add chapter ‘1.3 NeoPAC’.</td>
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<tr>
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<td>3. Add chapter ‘5.1.3 External LDO mode (NeoPAC)’.</td>
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<td>4. Add chapter ‘5.2.3 2.8V / 1.8V dual supply mode (NeoPAC)’</td>
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<td>5. Add chapter ‘5.3.3 2.8V signal supply Mode (NeoPAC)’.</td>
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<tr>
<td></td>
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<td>6. Modify chapter ‘9.3 Sensor exposure gain control’, 0x020E &amp; 0x020F description.</td>
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Important Notice

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1. Package Information

1.1 Bare die

![Bare die diagram (Top view)](image)

Table 1.1: Bare die pin description

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INT</td>
<td>Out</td>
<td>Interrupt output (Active High).</td>
</tr>
<tr>
<td>2</td>
<td>SDA</td>
<td>In/Out</td>
<td>Serial data I/O (Open drain).</td>
</tr>
<tr>
<td>3</td>
<td>SCL</td>
<td>In</td>
<td>I2C serial clock.</td>
</tr>
<tr>
<td>4</td>
<td>LVLD</td>
<td>Out</td>
<td>Line valid output.</td>
</tr>
<tr>
<td>5</td>
<td>FVLD</td>
<td>Out</td>
<td>Frame valid output.</td>
</tr>
<tr>
<td>6</td>
<td>TRIG</td>
<td>In</td>
<td>Frame trigger input (Internal pull down / Active high).</td>
</tr>
<tr>
<td>7</td>
<td>AGND</td>
<td>Ground</td>
<td>Analog ground.</td>
</tr>
<tr>
<td>8</td>
<td>AVDD</td>
<td>Power</td>
<td>Analog power (2.8V).</td>
</tr>
<tr>
<td>9</td>
<td>AGND</td>
<td>Ground</td>
<td>Analog ground.</td>
</tr>
<tr>
<td>10</td>
<td>DGND</td>
<td>Ground</td>
<td>Digital ground.</td>
</tr>
<tr>
<td>11</td>
<td>IOVDD</td>
<td>Power</td>
<td>IO power (1.8V/2.8V).</td>
</tr>
<tr>
<td>12</td>
<td>DVDD</td>
<td>Power</td>
<td>Digital power (1.5 V).</td>
</tr>
<tr>
<td>13</td>
<td>MCLK</td>
<td>In</td>
<td>Master clock input.</td>
</tr>
<tr>
<td>14</td>
<td>PCLKO / SCK</td>
<td>Out</td>
<td>Pixel clock / serial clock output.</td>
</tr>
<tr>
<td>15</td>
<td>D0 / SDO</td>
<td>Out</td>
<td>Data 0 output / Serial output.</td>
</tr>
<tr>
<td>16</td>
<td>D1</td>
<td>Out</td>
<td>Data 1 output.</td>
</tr>
<tr>
<td>17</td>
<td>D2</td>
<td>Out</td>
<td>Data 2 output.</td>
</tr>
<tr>
<td>18</td>
<td>D3</td>
<td>Out</td>
<td>Data 3 output.</td>
</tr>
<tr>
<td>19</td>
<td>D4</td>
<td>Out</td>
<td>Data 4 output.</td>
</tr>
<tr>
<td>20</td>
<td>D5</td>
<td>Out</td>
<td>Data 5 output.</td>
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<tr>
<td>21</td>
<td>DVDD</td>
<td>Power</td>
<td>Digital power (1.5 V).</td>
</tr>
<tr>
<td>22</td>
<td>DGND</td>
<td>Ground</td>
<td>Digital ground.</td>
</tr>
<tr>
<td>23</td>
<td>D6</td>
<td>Out</td>
<td>Data 6 output.</td>
</tr>
<tr>
<td>24</td>
<td>D7</td>
<td>Out</td>
<td>Data 7 output.</td>
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1.2 Chip scale package

**HM01B0-AWA**

![CSP pin diagram (Top view)](image)

**Figure 1.2: CSP pin diagram (Top view)**

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>A1</td>
<td>SDA</td>
<td>I/O</td>
<td>Serial Data I/O (Open Drain).</td>
</tr>
<tr>
<td>A2</td>
<td>INT</td>
<td>OUTPUT</td>
<td>Interrupt Output (Active High).</td>
</tr>
<tr>
<td>A3</td>
<td>D3</td>
<td>OUTPUT</td>
<td>Data 3 output.</td>
</tr>
<tr>
<td>A4</td>
<td>D2</td>
<td>OUTPUT</td>
<td>Data 2 output.</td>
</tr>
<tr>
<td>B1</td>
<td>LVLD</td>
<td>OUTPUT</td>
<td>Line valid output.</td>
</tr>
<tr>
<td>B2</td>
<td>SCL</td>
<td>INPUT</td>
<td>I2C serial clock.</td>
</tr>
<tr>
<td>B3</td>
<td>D1</td>
<td>OUTPUT</td>
<td>Data 1 output.</td>
</tr>
<tr>
<td>B4</td>
<td>D0/SDO</td>
<td>OUTPUT</td>
<td>Data 0 / Serial data output.</td>
</tr>
<tr>
<td>C1</td>
<td>TRIG</td>
<td>INPUT</td>
<td>Frame trigger input (Internal pull down active high).</td>
</tr>
<tr>
<td>C2</td>
<td>FVLD</td>
<td>OUTPUT</td>
<td>Frame valid output.</td>
</tr>
<tr>
<td>C3</td>
<td>PCLKO / SCK</td>
<td>OUTPUT</td>
<td>Pixel clock / serial clock output.</td>
</tr>
<tr>
<td>C4</td>
<td>MCLK</td>
<td>INPUT</td>
<td>Master clock input.</td>
</tr>
<tr>
<td>D1</td>
<td>AVDD</td>
<td>POWER</td>
<td>Analog power (2.8V).</td>
</tr>
<tr>
<td>D2</td>
<td>GND</td>
<td>GROUND</td>
<td>Ground.</td>
</tr>
<tr>
<td>D3</td>
<td>DVDD</td>
<td>POWER</td>
<td>Digital power (1.5 V).</td>
</tr>
<tr>
<td>D4</td>
<td>IOVDD</td>
<td>POWER</td>
<td>IO power (1.8V / 2.8V).</td>
</tr>
</tbody>
</table>

**Table 1.2: CSP pin description**
1.3 NeoPAC

![NeoPAC Diagram](image)

Figure 1.3: NeoPAC diagram (Top view)

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Pin name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INT</td>
<td>Out</td>
<td>Interrupt output (Active High).</td>
</tr>
<tr>
<td>2</td>
<td>SDA</td>
<td>In/Out</td>
<td>Serial data I/O (Open drain).</td>
</tr>
<tr>
<td>3</td>
<td>SCL</td>
<td>In</td>
<td>I2C serial clock.</td>
</tr>
<tr>
<td>4</td>
<td>LVLD</td>
<td>Out</td>
<td>Line valid output.</td>
</tr>
<tr>
<td>5</td>
<td>FVLD</td>
<td>Out</td>
<td>Frame valid output.</td>
</tr>
<tr>
<td>6</td>
<td>TRIG</td>
<td>In</td>
<td>Frame trigger input (Internal pull down / Active high).</td>
</tr>
<tr>
<td>7</td>
<td>AGND</td>
<td>Ground</td>
<td>Analog ground.</td>
</tr>
<tr>
<td>8</td>
<td>AVDD</td>
<td>Power</td>
<td>Analog power (2.8V).</td>
</tr>
<tr>
<td>9</td>
<td>AGND</td>
<td>Ground</td>
<td>Analog ground.</td>
</tr>
<tr>
<td>10</td>
<td>AGND</td>
<td>Ground</td>
<td>Analog ground.</td>
</tr>
<tr>
<td>11</td>
<td>DGND</td>
<td>Ground</td>
<td>Digital ground.</td>
</tr>
<tr>
<td>12</td>
<td>IOVDD</td>
<td>Power</td>
<td>IO power (1.8V/2.8V).</td>
</tr>
<tr>
<td>13</td>
<td>DVDD</td>
<td>Power</td>
<td>Digital power (1.5 V).</td>
</tr>
<tr>
<td>14</td>
<td>DVDD</td>
<td>Power</td>
<td>Digital power (1.5 V).</td>
</tr>
<tr>
<td>15</td>
<td>MCLK</td>
<td>In</td>
<td>Master clock input.</td>
</tr>
<tr>
<td>16</td>
<td>PCLKO / SCK</td>
<td>Out</td>
<td>Pixel Clock / Serial clock output.</td>
</tr>
<tr>
<td>17</td>
<td>D0 / SDO</td>
<td>Out</td>
<td>Data 0 output / Serial output.</td>
</tr>
<tr>
<td>18</td>
<td>D1</td>
<td>Out</td>
<td>Data 1 output.</td>
</tr>
<tr>
<td>19</td>
<td>D2</td>
<td>Out</td>
<td>Data 2 output.</td>
</tr>
<tr>
<td>20</td>
<td>D3</td>
<td>Out</td>
<td>Data 3 output.</td>
</tr>
<tr>
<td>21</td>
<td>D4</td>
<td>Out</td>
<td>Data 4 output.</td>
</tr>
<tr>
<td>22</td>
<td>D5</td>
<td>Out</td>
<td>Data 5 output.</td>
</tr>
<tr>
<td>23</td>
<td>DVDD</td>
<td>Power</td>
<td>Digital power (1.5 V).</td>
</tr>
<tr>
<td>24</td>
<td>DGND</td>
<td>Ground</td>
<td>Digital ground.</td>
</tr>
<tr>
<td>25</td>
<td>D6</td>
<td>Out</td>
<td>Data 6 output.</td>
</tr>
<tr>
<td>26</td>
<td>D7</td>
<td>Out</td>
<td>Data 7 output.</td>
</tr>
</tbody>
</table>

Table 1.3: NeoPAC pin description
2. Sensor Overview

The HM01B0 is an Ultra Low Power Image Sensor (ULPIS) that enables the integration of an “Always-on” camera for computer vision applications such as gestures, intelligent ambient light and proximity sensing, tracking and object identification. The unique architecture of the sensor enables the sensor to consume very low power of <4mW at QVGA 60FPS, <2mW at QVGA 30FPS, and <1.1mW at QQVGA 30FPS.

The HM01B0 contains 324 x 324 pixel resolutions and supports a 324 x 244 window mode which can be readout at a maximum frame rate of 60FPS, and a 2x2 monochrome binning mode with a maximum frame rate of 120FPS. The video data is transferred over a configurable 1-bit, 4-bit or 8-bit video interface with support for frame and line synchronization. The sensor integrates a black level calibration circuit, automatic exposure and gain control loop, self-oscillator and motion detection circuit with interrupt output to reduce host computation and commands to the sensor to optimize the system power consumption.

The sensor is available in a Chip Scale Package (CSP) or bare die and measures less than 5mm². The sensor supports single, dual or triple power supply configuration and requires only 3 passive components enabling a highly compact camera module design for devices such as IoT, wearable, smart building, smart phone, tablets and slim notebooks.

Figure 2.1: HM01B0 block diagram
3. Sensor Core and Function Description

3.1 Sensor array

The HM01B0 consists of an active pixel array of 324 columns and 324 rows. The sensor maximum effective resolution is 320 columns and 320 rows which include 4 border pixels.

For the sensors with color filter, the even numbered rows contain the Blue (B) and Green (G₁) pixel, and the odd numbered row contains the Red (R) and Green (G₂) pixels; the even numbered columns contain the Green (G₂) and Blue (B) pixels, and the odd column contains the Red (R) and Green (G₁) pixels. Optically black rows are used by the sensor for black level calibration. Programmable horizontal and vertical blanking time adjusts the line width and frame height, respectively.

![Column Readout Direction](default)

![Row Readout Direction](No Flip / No Mirror)

**Figure 3.1: Full resolution pixel readout (Monochrome)**

3.2 QVGA window readout

The QVGA sensor window with an active resolution of 324 x 244 pixels is programmed by setting register 0x3010[0] to 1. The location of the window is fixed such that the coordinate of the first pixel read out location is 0, 40.

![Set QVGA Sensor Window](X=0, Y=40)

**Figure 3.2: QVGA resolution pixel readout**
3.3 Monochrome QQVGA using pixel binning

QQVGA do not support the Bayer sensor version and only for the monochrome sensor version, 2 x 2 binning can be enabled to average 4 pixels in to 1 pixel which reduces resolution by a factor of four to QQVGA, and improves S/N ratio.

![Monochrome Full Frame Readout and Binning Readout](image)

**Figure 3.3: Monochrome full frame and binning readout mode**

3.4 Horizontal and vertical mirror

The sensor readout can be mirrored in the vertical and / or horizontal direction where the window center will remain unchanged. The horizontal and vertical mirror readout can be applied in Full, QQVGA, and binning mode.

In the color sensor version, the color of the first pixel read out will change according to the selected mirror mode as shown in the figure below.

![Horizontal and Vertical Mirror Modes](image)

**Figure 3.4: Horizontal and vertical mirror readout modes**
4. Image Signal Processor Functional Description

The sensor ISP features can be configured by the host through the serial register interface. Please contact Himax Imaging for application notes and information.

![Figure 4.1: ISP blocks](image-url)
<table>
<thead>
<tr>
<th>Block acronym</th>
<th>Block name</th>
<th>Description</th>
<th>Register range</th>
<th>Register enable bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP</td>
<td>Test Pattern</td>
<td>Two test patterns are supported (See figure below): a. Walking 1's b. Color bar</td>
<td>0x0601</td>
<td>0x0601[0]</td>
</tr>
<tr>
<td>BLC</td>
<td>Black Level Correction</td>
<td>Adjusts the black level of the frame to the target programmed value based on optical black pixel data</td>
<td>0x1003 0x1007</td>
<td>0x1000[0] 0x1006[0]</td>
</tr>
<tr>
<td>DIG GAIN</td>
<td>Digital Gain</td>
<td>Global digital gain applied to the video data. Programmed in 2.6 format (2-bit integer, 6-bit floating)</td>
<td>0x020E 0x020F</td>
<td>-</td>
</tr>
<tr>
<td>DPC</td>
<td>Defective Pixel Correction</td>
<td>Correct single hot and cold pixel using neighboring “good” pixel data. Selectable for monochrome and Bayer.</td>
<td>0x100B 0x100C</td>
<td>0x1008[2:0]</td>
</tr>
<tr>
<td>STAT_MD</td>
<td>Statistics</td>
<td>6 or 8-bit average motion statistics for programmable window</td>
<td>0x2011 ~ 0x2018</td>
<td>0x2000[2:1]</td>
</tr>
<tr>
<td>AEG</td>
<td>Automatic Exposure Gain</td>
<td>Control loop which adjusts the sensor exposure, analog and digital gain to the user-defined target luminance value. The AEG can be programmed to avoid 50Hz and 60Hz flicker.</td>
<td>0x2101 ~ 0x2113</td>
<td>0x2100[0]</td>
</tr>
<tr>
<td>MD</td>
<td>Motion Detection</td>
<td>Detect for presence of motion within programmable Motion Region of Interest (separate statistics from AEC). The status of the motion detection, including triggered interrupt can be accessed through the registers.</td>
<td>0x2153 ~ 0x215B</td>
<td>0x2150[0]</td>
</tr>
</tbody>
</table>

Table 4.1: Digital ISP block

Figure 4.2: Test image patterns
5. Typical Application Circuit

5.1 Triple supply

5.1.1 External LDO mode (Bare die)

Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) 4-bit data format will output data on D0 ~ D3.
(3) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
(4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.1: Triple supply (2.8V / 1.8V / 1.5V) application circuit for bare die
5.1.2 External LDO mode (CSP)

Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.

Figure 5.2: Triple supply (2.8V / 1.8V / 1.5V) application circuit for CSP
5.1.3 External LDO mode (NeoPAC)

Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) 4-bit data format will output data on D0 ~ D3.
(3) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
(4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.3: Triple supply (2.8V / 1.8V / 1.5V) application circuit for NeoPAC
5.2 Dual supply

5.2.1 2.8V / 1.8V dual supply mode (Bare die)

Note:

1. Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
2. 4-bit data format will output data on D0 ~ D3.
3. Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
4. Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.4: Dual supply (2.8V / 1.8V) application circuit for bare die
### 5.2.2 2.8V / 1.8V dual supply mode (CSP)

![Diagram of dual supply (2.8V / 1.8V) application circuit for CSP](image)

**Note:**
1. Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
2. Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.

**Figure 5.5:** Dual supply (2.8V / 1.8V) application circuit for CSP
5.2.3 2.8V / 1.8V dual supply mode (NeoPAC)

**Note:**
1. Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
2. 4-bit data format will output data on D0 ~ D3.
3. Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
4. Analog ground and digital ground should be kept separate and connected to a single point outside the module.

*Figure 5.6: Dual supply (2.8V / 1.8V) application circuit for NeoPAC*
5.3 Single supply

5.3.1 2.8V signal supply mode (Bare die)

![Single supply 2.8V application circuit for bare die]

**Note:**
1. Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
2. 4-bit data format will output data on D0 ~ D3.
3. Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
4. Analog ground and digital ground should be kept separate and connected to a single point outside the module.

*Figure 5.7: Single supply 2.8V application circuit for bare die*
5.3.2 2.8V signal supply Mode (CSP)

**Note:**
(1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.

**Figure 5.8:** Single supply 2.8V application circuit for CSP
5.3.3 2.8V signal supply Mode (NeoPAC)

Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) 4-bit data format will output data on D0 ~ D3.
(3) Pull-up resistor of 4.7kΩ to correct I/O voltage is recommended for SDA / SCL.
(4) Analog ground and digital ground should be kept separate and connected to a single point outside the module.

Figure 5.9: Single supply 2.8V application circuit for NeoPAC
6. System Level Description

6.1 Operating modes

The HM01B0 supports five modes of operation as shown in the table below.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Description</th>
<th>Power</th>
<th>Register values</th>
<th>I2C</th>
<th>CLOCK</th>
<th>Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power off</td>
<td>No power supplied to sensor</td>
<td>Off</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>S/W standby</td>
<td>Low-power consumption, no video</td>
<td>On</td>
<td>Retained</td>
<td>On</td>
<td>On or Off</td>
<td>Standby</td>
</tr>
<tr>
<td>Streaming 1</td>
<td>Mode_select [2:0]=001 I2C triggered streaming</td>
<td>On</td>
<td>Retained</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td></td>
<td>enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Streaming 2</td>
<td>Mode_select [2:0]=011 I2C triggered frame; output</td>
<td>On</td>
<td>Retained</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td></td>
<td>register programmed number of frames(0x3020[7:0]),</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>then enters s/w standby and clears Mode_select</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>register bit to 000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Streaming 3</td>
<td>Mode_select [2:0]=101 Digital input pin (TRIG)</td>
<td>On</td>
<td>Retained</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td></td>
<td>frame trigger</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 6.1: Operating modes

Figure 6.1: State diagram (I2C trigger)
The HM01B0 supports hardware trigger mode. The user can control the sensor to stream on/off by setting “TRIG” pin high/low. This operating mode can also be used to synchronize multiple HM01B0 sensors if all the sensors have a common master clock input (MCLK). The parallel interfaces of all the sensors are exactly synchronized and the user can use the pixel clock of one sensor to latch other’s sensor data.

### Output Format

<table>
<thead>
<tr>
<th>Format</th>
<th>Mode</th>
<th>MCLK (MHz)</th>
<th>Sensor_Core (MHz)</th>
<th>Sensor_Register (MHz)</th>
<th>PCLKO (MHz)</th>
<th>Maximum FPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit</td>
<td>SYNC</td>
<td>3-24</td>
<td>MCLK/2.4</td>
<td>MCLK</td>
<td>Sensor_Core</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>Non-SYNC</td>
<td>3-36</td>
<td>MCLK/2.4</td>
<td>MCLK/1,2,4,8</td>
<td>Sensor_Core</td>
<td>60</td>
</tr>
<tr>
<td>4-bit</td>
<td>SYNC</td>
<td>3-24</td>
<td>MCLK/2.4</td>
<td>MCLK</td>
<td>2x Sensor_Core</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td>Non-SYNC</td>
<td>3-36</td>
<td>MCLK/2.4</td>
<td>MCLK/1,2,4,8</td>
<td>2x Sensor_Core</td>
<td>60</td>
</tr>
<tr>
<td>1-bit</td>
<td>SYNC</td>
<td>3-36</td>
<td>MCLK/8</td>
<td>MCLK</td>
<td>MCLK</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>Non-SYNC</td>
<td>3-36</td>
<td>MCLK/8</td>
<td>MCLK/1,2,4,8</td>
<td>MCLK</td>
<td>45</td>
</tr>
</tbody>
</table>

#### Table 6.2: MCLK configuration for SYNC and non-SYNC mode

**6.2 Reset**

The HM01B0 provides two methods of reset methods: Power On Reset (POR) and software reset.

During power up, an internal POR circuit applies a system reset until the DVDD supply reaches a monitored voltage threshold. This insures that the supply voltage is stable and the sensor is properly initialized.

Software reset is applied by writing register value 0 or 1 to register bit SW_RESET[0] (0x0103[0]). When reset is applied, the sensor will return to “Standby Mode” and reset all serial interface registers to its default values.
6.3 Power up sequence

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t1</td>
<td>AVDD to IOVDD</td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>t2</td>
<td>IOVDD to DVDD</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>tPOR</td>
<td>Power On Reset time</td>
<td>50</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 6.3: Power up sequence timing
6.4 Clock setup

Reference clock to the sensor can be provided externally through the MCLK pin, or generated by the on-chip self-oscillator. The sensor will automatically select the self-oscillator when the reference clock is not present at the MCLK pin.

- The self-oscillator is only used for motion detection and doesn’t care that much on flicker.
- The frequency for Sensor_Core and Sensor_Register are 1/8*MCLK in self-oscillator mode.

6.4.1 MCLK and self-oscillator mode switch

- The Register 0x3067[0] set to 1 before MCLK off for MCLK mode to self oscillator mode.
- The Register 0x3067[0] set to 0 before self oscillator mode off for self oscillator mode to MCLK mode.
6.5 IO control options

Options for IO pins can be programmed based on the following table. Please consult Himax Imaging FAE for additional information.

<table>
<thead>
<tr>
<th>Output pin</th>
<th>Drive strength control</th>
<th>Polarity</th>
<th>Interface bit width</th>
<th>Sync advance</th>
<th>MSB / LSB</th>
<th>PCLKO clock gating</th>
</tr>
</thead>
<tbody>
<tr>
<td>D[7:4]</td>
<td>-</td>
<td>-</td>
<td>0x3059[6:5]</td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>D[3:1]</td>
<td>0x3063[2:0]</td>
<td>-</td>
<td>0x3023 [4:0]</td>
<td></td>
<td>0=MSB</td>
<td>-</td>
</tr>
<tr>
<td>D[0]</td>
<td>0x3062[6:4]</td>
<td>-</td>
<td>0x3022 [3:0]</td>
<td></td>
<td>1=LSB</td>
<td>-</td>
</tr>
<tr>
<td>LVLD</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>FVLD</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>PCLKO</td>
<td>0x3062[2:0]</td>
<td>0x3060[0]</td>
<td></td>
<td></td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>INT</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td>-</td>
</tr>
</tbody>
</table>

Note: (1) 1-bit / 4-bit data mode only.

Table 6.4: IO control options

The status for output pins in standby/streaming mode can be control by register 0x3065[1:0]

<table>
<thead>
<tr>
<th>Register 0x3065[1:0]</th>
<th>Pin</th>
<th>Standby mode</th>
<th>Streaming mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output pins</td>
<td>Hi-z</td>
<td>Driving</td>
</tr>
<tr>
<td></td>
<td>INT</td>
<td>Hi-z</td>
<td>Driving</td>
</tr>
<tr>
<td>1</td>
<td>Output pins</td>
<td>Hi-z</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td>INT</td>
<td>Hi-z</td>
<td>Driving</td>
</tr>
<tr>
<td>2</td>
<td>Output pins</td>
<td>Hi-z</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td>INT</td>
<td>Hi-z</td>
<td>Driving</td>
</tr>
<tr>
<td>3</td>
<td>Output pins</td>
<td>Hi-z</td>
<td>Hi-z</td>
</tr>
<tr>
<td></td>
<td>INT</td>
<td>Hi-z</td>
<td>Driving</td>
</tr>
</tbody>
</table>

Table 6.5: Output pin status

![Non-gated and gated serial data clock option](image)

Figure 6.5: Non-gated and gated serial data clock option
6.6 Data format control

The HM01B0 supports RAW8 and RAW6 data format. The default is 8-bit data format, and 6-bit data format is selected by setting register bit DATAFORMAT 0x3011 [0] = 1.
Figure 6.7: 6-bit and 8-bit RAW output format on 4-bit data IO interface

Figure 6.8: RAW output format on serial data IO interface
7. Serial Interface Description

The 2-wire serial interface provides read/write access to the sensor registers:

- 2-wire serial interface consists of SDA (Bidirectional serial data) and SCL (Serial clock) pins.
- HM01B0 uses 16-bit register address and 8-bit register data.
- The sensor uses double-buffered registers to ensure that register changes that affect sensor operation takes place at the beginning of the next valid video frame.
- The host generates SCL clock signal to the sensor and uses the signal to synchronize all data transfer.

7.1 I2C slave address ID

- The address of the sensor is 0x24.
- The address of the sensor can be changed by register 0x3401[6:0] when register 0x3400[0] set to 1. The address of the sensor get restored back to default (0x24) after rebooting.

7.2 Start / Stop conditions

The start and stop conditions on the serial bus is issued by the Host.

<table>
<thead>
<tr>
<th>SDA Transition</th>
<th>SCL</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>High to Low</td>
<td>High</td>
<td>Start</td>
</tr>
<tr>
<td>Low to High</td>
<td>High</td>
<td>Stop</td>
</tr>
</tbody>
</table>

Table 7.1: Serial interface start and stop transition

![Start (S) and Stop (P)](image)

Figure 7.1: 2-wire serial interface start and stop condition

7.3 Data valid

One SCL pulse is generated for each data bit transferred. The host should ensure that the SDA signal must be stable when SCL in High. The SDA signal can transition when SCL is Low.

7.4 Data format

Data is transferred one byte at a time. The most significant bit should always be transferred first. Each byte is followed by an acknowledgement (ACK) or a no-acknowledgement bit (No ACK).
7.5 Acknowledge / No acknowledgement

Each 8-bit is followed by an Acknowledge (ACK) or No-Acknowledge (No ACK) bit.

- Acknowledge: The Host will release the SDA line. The sensor will drive the SDA line low.
- No-Acknowledge: The Host will release the SDA line. The sensor will not drive the SDA pin (Pulled high). The No-Ack bit is used to terminate a read sequence.

7.6 Write sequence

The write sequence is initiated by the Host with Start (S) condition, followed by 8-bit device slave ID (write ID)

- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address (high byte first, then low byte), then the register data. After each byte, the sensor will issue an ACK or NO ACK signal.
- The write operation is completed when the Host asserts a stop condition.

![Figure 7.2: 2-wire serial interface 16-bit address write](image)

7.7 Read sequence

The read sequence is initiated by Host with Start (S) condition, followed by the 8-bit device slave ID (write ID).

- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address (high byte first, then low byte), then the register data. After each byte, the sensor will issue an ACK or NO ACK bit.
- The write operation is completed when the Host asserts a Stop condition.
- The Host must issue another Start condition, followed by the 8-bit device slave ID (Read ID).
- If the register ID is recognized by the sensor, the ACK bit will be sent to the Host.
- The sensor will respond with the Register Data Out.
- The Host will issue an ACK, and then asserts the Stop condition.

![Figure 7.3: 2-wire serial interface 16-bit address read](image)
8. Sensor Core Control

8.1 Frame retiming

Serial registers that are synchronized to sensor timing utilize double-buffer register to ensure that changes take effect at the start of the frame boundary. In the Register Table section of this document, the registers that require retiming, such as gain and integration (exposure), are indicated by the designator CMU (Command Update).

Changes to retimed registers take effect at the boundary of the second subsequent frame (N+2) as shown in the figure below. When the register 0x3035 [7] is set to 1, both analogy and digital gain can be applied at frame N+1 if no other CMU register settings are updated within the same retiming cycle.

![Figure 8.1: (N+2) command update (CMU) timing](image)

8.2 Analog gain control

Analog gain follows the equation $2^N$ where N is set by ANALOG_GLOBAL_GAIN 0x0205 [6:4]. The valid programmable values for the analog gain register are defined in table below.

<table>
<thead>
<tr>
<th>Code (hex)</th>
<th>Gain (x)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0x10</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td>0x20</td>
<td>4</td>
<td>12</td>
</tr>
<tr>
<td>0x30</td>
<td>8</td>
<td>18</td>
</tr>
</tbody>
</table>

Table 8.1: Global analog gain settings

8.3 Suggestion for analog gain and digital gain

- Analogy gain x digital gain $\leq 16x$ for machine version
- Analogy gain x digital gain $\leq 8x$ for human version
8.4 Exposure control

The HM01B0 supports coarse integration control with a programmable resolution of 1 row. The minimum integration time is 2 rows. The exposure time of the sensor is calculated using the following equation:

A. Integration time (seconds) = coarse_integration x line_length_pck / vt_pix_clk (MHz) x 1 x 10^6
B. Coarse_integration_time ≤ (frame_length_lines − 2)

8.4.1 50Hz / 60Hz flicker avoidance

To avoid flicker, the sensor exposure time should be set in intervals of 1/100 seconds or 1/120 seconds for 50Hz or 60Hz flicker avoidance, respectively.

A. Integration Step Size (60Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 120
B. Integration Step Size (50Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 100

8.5 Frame rate control

The frame rate of the sensor is calculated based on the Video Timing Clock and uses the following equations:

A. 65535 ≥ line_length_pck ≥ min_line_length_pck
B. 65535 ≥ frame_length_lines ≥ min_frame_length_lines
C. frame rate = vt_pix_clk (MHz) x 1 x 10^6 / (frame_length_lines x line_length_pck)

<table>
<thead>
<tr>
<th>Minimum value</th>
<th>Full frame</th>
<th>QVGA</th>
<th>QQVGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>min_line_length_pck</td>
<td>0x0178</td>
<td>0x0178</td>
<td>0x00D7</td>
</tr>
<tr>
<td>min_frame_length_lines</td>
<td>0x0158</td>
<td>0x0104</td>
<td>0x0080</td>
</tr>
</tbody>
</table>

Table 8.2: Constraint for line length and frame length
## 9. Register Table

### 9.1 Sensor ID

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>[7:0]</td>
<td>MODE_ID_H [15:8]</td>
<td>RO</td>
<td>16-bit sensor Part number (HM01B0)</td>
<td>-</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0001</td>
<td>[7:0]</td>
<td>MODE_ID_L [7:0]</td>
<td>RO</td>
<td></td>
<td>-</td>
<td>0xB0</td>
</tr>
<tr>
<td>0x0002</td>
<td>[7:0]</td>
<td>SILICON_REV</td>
<td>RO</td>
<td>Silicon Revision Number</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>0x0005</td>
<td>[7:0]</td>
<td>FRAME_COUNT</td>
<td>RO</td>
<td>Frame counter</td>
<td>-</td>
<td>0xFF</td>
</tr>
<tr>
<td>0x0006</td>
<td>[7:0]</td>
<td>PIXEL_ORDER</td>
<td>RO</td>
<td>[1:0] Color Sensor Pixel Order</td>
<td></td>
<td>0x02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 – GR</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – RG</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2 – BG</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3 – GB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 9.2 Sensor mode control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0100</td>
<td>[2:0]</td>
<td>MODE_SELECT</td>
<td>RW</td>
<td>[2:0] Sensor mode selection</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>000: Standby</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>001: Streaming</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>011: Streaming 2 (Output N frames)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>101: Streaming 3 (Hardware Trigger)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0101</td>
<td>[1:0]</td>
<td>IMAGE_ORIENTATION</td>
<td>RW</td>
<td>Image Orientation</td>
<td>Y</td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[0]: Horizontal Mirror Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[1]: Vertical Flip Enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0103</td>
<td>[0]</td>
<td>SW_RESET</td>
<td>W</td>
<td>software reset</td>
<td>-</td>
<td>0xFF</td>
</tr>
<tr>
<td>0x0104</td>
<td>[0]</td>
<td>GRP_PARAM_HOLD</td>
<td>W</td>
<td>Group parameter hold</td>
<td>-</td>
<td>0xFF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 – consume</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 – hold</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 9.3 Sensor exposure gain control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0202</td>
<td>[7:0]</td>
<td>INTEGRATION_H [15:8]</td>
<td>RW</td>
<td>Coarse integration time in lines (16-bit UINT)</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0203</td>
<td>[7:0]</td>
<td>INTEGRATION_L [7:0]</td>
<td>RW</td>
<td></td>
<td>Y</td>
<td>0x08</td>
</tr>
<tr>
<td>0x0205</td>
<td>[6:4]</td>
<td>ANALOG_GAIN</td>
<td>RW</td>
<td>Analog Global Gain code (8-bit UINT)</td>
<td>Y</td>
<td>0x00</td>
</tr>
<tr>
<td>0x020E</td>
<td>[1:0]</td>
<td>DIGITAL_GAIN_H [9:8]</td>
<td>RW</td>
<td>Digital Global Gain code (8-bit UINT)</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x020F</td>
<td>[7:2]</td>
<td>DIGITAL_GAIN_L [7:2]</td>
<td>RW</td>
<td></td>
<td>Y</td>
<td>0x00</td>
</tr>
</tbody>
</table>
## 9.4 Frame timing control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0340</td>
<td>[7:0]</td>
<td>FRAME_LENGTH_LINES_H [15:8]</td>
<td>RW</td>
<td>frame_length_lines (16-bit UINT)</td>
<td>Y</td>
<td>0x02</td>
</tr>
<tr>
<td>0x0341</td>
<td>[7:0]</td>
<td>FRAME_LENGTH_LINES_L [7:0]</td>
<td>RW</td>
<td></td>
<td>Y</td>
<td>0x32</td>
</tr>
<tr>
<td>0x0342</td>
<td>[7:0]</td>
<td>LINE_LENGTH_PCK_H [15:8]</td>
<td>RW</td>
<td>line_length_pck (16-bit UINT)</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0343</td>
<td>[7:0]</td>
<td>LINE_LENGTH_PCK_L [7:0]</td>
<td>RW</td>
<td></td>
<td>Y</td>
<td>0x72</td>
</tr>
</tbody>
</table>

## 9.5 Binning mode control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0381</td>
<td>[0]</td>
<td>Reserved</td>
<td>RW</td>
<td>Set to 1</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0383</td>
<td>[1:0]</td>
<td>Readout_x</td>
<td>RW</td>
<td>Readout for x [1:0] : 1 : full 3 : Horizontal BIN2 timing enable</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0385</td>
<td>[0]</td>
<td>Reserved</td>
<td>RW</td>
<td>Set to 1</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0387</td>
<td>[1:0]</td>
<td>Readout_y</td>
<td>RW</td>
<td>Readout for y [1:0] : 1 : full 3 : Vertical BIN2 timing enable</td>
<td>Y</td>
<td>0x01</td>
</tr>
<tr>
<td>0x0390</td>
<td>[1:0]</td>
<td>BINNING_MODE</td>
<td>RW</td>
<td>[0] Vertical Binning [1] Horizontal Binning</td>
<td>Y</td>
<td>0x00</td>
</tr>
</tbody>
</table>

## 9.6 Test pattern control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0601</td>
<td>[7:0]</td>
<td>TEST_PATTERN_MODE</td>
<td>RW</td>
<td>Test Pattern Mode [0] : test pattern enable [4] : mode selection 0 : color bar 1 : walking 1</td>
<td>-</td>
<td>0x00</td>
</tr>
</tbody>
</table>

## 9.7 Black level control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1000</td>
<td>[7:0]</td>
<td>BLC_CFG</td>
<td>RW</td>
<td>blc configuration [0] : blc en</td>
<td>-</td>
<td>0x01</td>
</tr>
<tr>
<td>0x1003</td>
<td>[7:0]</td>
<td>BLC_TGT</td>
<td>RW</td>
<td>Black level target 0-255</td>
<td>-</td>
<td>0x20</td>
</tr>
<tr>
<td>0x1006</td>
<td>[0]</td>
<td>BLC_EN</td>
<td>RW</td>
<td>BLI enable</td>
<td>-</td>
<td>0x00</td>
</tr>
<tr>
<td>0x1007</td>
<td>[7:0]</td>
<td>BLC2_TGT</td>
<td>RW</td>
<td>BLC2 target, set to the same level as BLC target</td>
<td>-</td>
<td>0x20</td>
</tr>
</tbody>
</table>
# 9.8 Sensor reserved

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1008</td>
<td>[7:0]</td>
<td>DPC_CTRL</td>
<td>RW</td>
<td>DPC control</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[2:0] : DPC option</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: dpc off</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: option1- mono</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3: option1- bayer</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5: option2- bayer</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[3]: boundary bypass enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x100B</td>
<td>[7:0]</td>
<td>SINGLE_THR_HOT</td>
<td>RW</td>
<td>Single hot pixel threshold</td>
<td></td>
<td>0xFF</td>
</tr>
<tr>
<td>0x100C</td>
<td>[7:0]</td>
<td>SINGLE_THR_COLD</td>
<td>RW</td>
<td>Single cold pixel threshold</td>
<td></td>
<td>0xFF</td>
</tr>
</tbody>
</table>

# 9.9 VSYNC, HSYNC and pixel shift register

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1012</td>
<td>[2:0]</td>
<td>VSYNC_HSYNC_PIX_EL_SHIFT_EN</td>
<td>RW</td>
<td>Shifting enable</td>
<td></td>
<td>0x07</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[0]: vsync shift enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[1]: hsync shift enable</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[2]: pixel shift enable</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# 9.10 Statistic control and read only

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2000</td>
<td>[7:0]</td>
<td>STATISTIC_CTRL</td>
<td>RW</td>
<td>ROI statistic control</td>
<td></td>
<td>0x07</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[0] : AE stat en</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[1] : MD LROI stat en</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[2] : Set to 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[4] : Ave. 8/16 frame select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2011</td>
<td>[0]</td>
<td>MD_LROI_X_START_H</td>
<td>RW</td>
<td>motion detection LROI (x start High Byte)</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2012</td>
<td>[7:0]</td>
<td>MD_LROI_X_START_L</td>
<td>RW</td>
<td>motion detection LROI (x start Low Byte)</td>
<td></td>
<td>0x48</td>
</tr>
<tr>
<td>0x2013</td>
<td>[0]</td>
<td>MD_LROI_Y_START_H</td>
<td>RW</td>
<td>motion detection LROI (y start High Byte)</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2014</td>
<td>[7:0]</td>
<td>MD_LROI_Y_START_L</td>
<td>RW</td>
<td>motion detection LROI (y start Low Byte)</td>
<td></td>
<td>0x70</td>
</tr>
<tr>
<td>0x2015</td>
<td>[0]</td>
<td>MD_LROI_X_END_H</td>
<td>RW</td>
<td>motion detection LROI (x end High Byte)</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2016</td>
<td>[7:0]</td>
<td>MD_LROI_X_END_L</td>
<td>RW</td>
<td>motion detection LROI (x end Low Byte)</td>
<td></td>
<td>0xDB</td>
</tr>
<tr>
<td>0x2017</td>
<td>[0]</td>
<td>MD_LROI_X_END_H</td>
<td>RW</td>
<td>motion detection LROI (y end High Byte)</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2018</td>
<td>[7:0]</td>
<td>MD_LROI_X_END_L</td>
<td>RW</td>
<td>motion detection LROI (y end Low Byte)</td>
<td></td>
<td>0xB3</td>
</tr>
</tbody>
</table>
### 9.11 Automatic exposure gain control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2100</td>
<td>[7:0]</td>
<td>AE_CTRL</td>
<td>RW</td>
<td>AE Control loop enable [0] : AE en</td>
<td></td>
<td>0x01</td>
</tr>
<tr>
<td>0x2101</td>
<td>[7:0]</td>
<td>AE_TARGET_MEAN</td>
<td>RW</td>
<td>AE target mean</td>
<td></td>
<td>0x3C</td>
</tr>
<tr>
<td>0x2102</td>
<td>[7:0]</td>
<td>AE_MIN_MEAN</td>
<td>RW</td>
<td>AE min mean</td>
<td></td>
<td>0x0A</td>
</tr>
<tr>
<td>0x2103</td>
<td>[7:0]</td>
<td>CONVERGE_IN_TH</td>
<td>RW</td>
<td>Converge in threshold</td>
<td></td>
<td>0x03</td>
</tr>
<tr>
<td>0x2104</td>
<td>[7:0]</td>
<td>CONVERGE_OUT_T H</td>
<td>RW</td>
<td>Converge out threshold</td>
<td></td>
<td>0x05</td>
</tr>
<tr>
<td>0x2105</td>
<td>[7:0]</td>
<td>MAX_INTG_H</td>
<td>RW</td>
<td>Maximum INTG High Byte</td>
<td></td>
<td>0x01</td>
</tr>
<tr>
<td>0x2106</td>
<td>[7:0]</td>
<td>MAX_INTG_L</td>
<td>RW</td>
<td>Maximum INTG Low Byte</td>
<td></td>
<td>0x54</td>
</tr>
<tr>
<td>0x2107</td>
<td>[7:0]</td>
<td>MIN_INTG</td>
<td>RW</td>
<td>Minimum INTG</td>
<td></td>
<td>0x02</td>
</tr>
<tr>
<td>0x2108</td>
<td>[7:0]</td>
<td>MAX_AGAIN_FULL</td>
<td>RW</td>
<td>Maximum Analog gain in full frame mode</td>
<td></td>
<td>0x03</td>
</tr>
<tr>
<td>0x2109</td>
<td>[7:0]</td>
<td>MAX_AGAIN_BIN2</td>
<td>RW</td>
<td>Maximum Analog gain in bin2 mode</td>
<td></td>
<td>0x04</td>
</tr>
<tr>
<td>0x210A</td>
<td>[7:0]</td>
<td>MIN_AGAIN</td>
<td>RW</td>
<td>Minimum Again</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x210B</td>
<td>[7:0]</td>
<td>MAX_DGAIN</td>
<td>RW</td>
<td>Maximum Dgain</td>
<td></td>
<td>0x0C</td>
</tr>
<tr>
<td>0x210C</td>
<td>[7:0]</td>
<td>MIN_DGAIN</td>
<td>RW</td>
<td>Minimum Dgain</td>
<td></td>
<td>0x40</td>
</tr>
<tr>
<td>0x210D</td>
<td>[7:0]</td>
<td>DAMPING_FACTOR</td>
<td>RW</td>
<td>Damping factor</td>
<td></td>
<td>0x20</td>
</tr>
<tr>
<td>0x210E</td>
<td>[7:0]</td>
<td>FS_CTRL</td>
<td>RW</td>
<td>Flicker Step control [0] : FS en [1] : frequency selection 0 : 50Hz 1 : 60Hz</td>
<td></td>
<td>0x03</td>
</tr>
<tr>
<td>0x210F</td>
<td>[7:0]</td>
<td>FS_60HZ_H</td>
<td>RW</td>
<td>Flicker Step 60Hz parameter High Byte</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2110</td>
<td>[7:0]</td>
<td>FS_60HZ_L</td>
<td>RW</td>
<td>Flicker Step 60Hz parameter Low Byte</td>
<td></td>
<td>0x3C</td>
</tr>
<tr>
<td>0x2111</td>
<td>[7:0]</td>
<td>FS_50HZ_H</td>
<td>RW</td>
<td>Flicker Step 50Hz parameter High Byte</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2112</td>
<td>[7:0]</td>
<td>FS_50HZ_L</td>
<td>RW</td>
<td>Flicker Step 50Hz parameter Low Byte</td>
<td></td>
<td>0x32</td>
</tr>
<tr>
<td>0x2113</td>
<td>[7:0]</td>
<td>FS_HYST_TH</td>
<td>RW</td>
<td>Flicker Step hysteresis threshold</td>
<td></td>
<td>0x66</td>
</tr>
</tbody>
</table>

### 9.12 Motion detection control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2150</td>
<td>[7:0]</td>
<td>MD_CTRL</td>
<td>RW</td>
<td>Motion Detection control [0] : MD LROI en [1] : Set to 1</td>
<td></td>
<td>0x03</td>
</tr>
<tr>
<td>0x2153</td>
<td>[0]</td>
<td>I2C_CLEAR</td>
<td>W</td>
<td>I2c clear</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x2155</td>
<td>[7:0]</td>
<td>WMEAN_DIFF_TH_H</td>
<td>RW</td>
<td>wMean difference threshold H</td>
<td></td>
<td>0x7D</td>
</tr>
<tr>
<td>0x2156</td>
<td>[7:0]</td>
<td>WMEAN_DIFF_TH_M</td>
<td>RW</td>
<td>wMean difference threshold M</td>
<td></td>
<td>0x4B</td>
</tr>
<tr>
<td>0x2157</td>
<td>[7:0]</td>
<td>WMEAN_DIFF_TH_L</td>
<td>RW</td>
<td>wMean difference threshold L</td>
<td></td>
<td>0x05</td>
</tr>
<tr>
<td>0x2158</td>
<td>[7:0]</td>
<td>MD_THH</td>
<td>RW</td>
<td>MD threshold H</td>
<td></td>
<td>0x80</td>
</tr>
<tr>
<td>0x2159</td>
<td>[7:0]</td>
<td>MD_THM1</td>
<td>RW</td>
<td>MD threshold M1</td>
<td></td>
<td>0x32</td>
</tr>
<tr>
<td>0x215A</td>
<td>[7:0]</td>
<td>MD_THM2</td>
<td>RW</td>
<td>MD threshold M2</td>
<td></td>
<td>0x19</td>
</tr>
<tr>
<td>0x215B</td>
<td>[5:0]</td>
<td>MD_THL</td>
<td>RW</td>
<td>MD threshold L</td>
<td></td>
<td>0x03</td>
</tr>
</tbody>
</table>
9.13 Sensor timing control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3010</td>
<td>7:0</td>
<td>QVGA_WIN_EN</td>
<td>RW</td>
<td>[0] : QVGA enable</td>
<td>Y</td>
<td>0x00</td>
</tr>
<tr>
<td>0x3011</td>
<td>6:0</td>
<td>SIX_BIT_MODE_EN</td>
<td>RW</td>
<td>[0] : 6 bit mode enable [6:4] : Reserved</td>
<td></td>
<td>0x70</td>
</tr>
<tr>
<td>0x3020</td>
<td>7:0</td>
<td>PMU_PROGRAMMABLE_FRAMECNT</td>
<td>RW</td>
<td>PMU AutoSleep Framecnt</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3022</td>
<td>4:0</td>
<td>ADVANCE_VSYNC</td>
<td>RW</td>
<td>Advance VSYNC field from 0 to 20 (1LSB=1 Row period)</td>
<td></td>
<td>0x02</td>
</tr>
<tr>
<td>0x3023</td>
<td>5:0</td>
<td>ADVANCE_HSYNC</td>
<td>RW</td>
<td>Advance Hsync field from 0 to 20 (1LSB=1 Pixel Clock)</td>
<td></td>
<td>0x02</td>
</tr>
<tr>
<td>0x3035</td>
<td>7</td>
<td>EARLY_GAIN</td>
<td>RW</td>
<td>Applies gain in N+1 frame if Integration is not updated in the same CMU frame</td>
<td></td>
<td>0xF3</td>
</tr>
</tbody>
</table>

9.14 IO and clock control

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3061</td>
<td>7:0</td>
<td>ANA_Register_11</td>
<td>RW</td>
<td>[3:1] : ldo_stb_d [5] : main LDO power down enable</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3062</td>
<td>7:0</td>
<td>IO_DRIVE_STR</td>
<td>RW</td>
<td>IO drive strength control [3:0] : PCLKO [7:4] : D[0]</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3063</td>
<td>3:0</td>
<td>IO_DRIVE_STR2</td>
<td>RW</td>
<td>IO drive strength control [3:0] : D[3:1]</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3064</td>
<td>2</td>
<td>ANA_Register_14</td>
<td>RW</td>
<td>Trigger SYNC mode enable [2] : Trigger SYNC mode enable</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3065</td>
<td>1:0</td>
<td>OUTPUT_PIN_STATU S_CONTROL</td>
<td>RW</td>
<td>Output pin status control [1:0]</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3067</td>
<td>1:0</td>
<td>ANA_Register_17</td>
<td>RW</td>
<td>[0] : OSC MCLK switch 0 : OSC mode en 1 : MCLK mode en [1] : Trigger signal sync with MCLK polarity 0 : rising edge 1 : falling edge</td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td>0x3068</td>
<td>0</td>
<td>PCLK_POLARITY</td>
<td>RW</td>
<td>PCLKO Polarity [0] : pclk_polarity 0 : rising edge 1 : falling edge [7:4]: Reserved</td>
<td></td>
<td>0x20</td>
</tr>
</tbody>
</table>
9.15 I2C slave registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Byte</th>
<th>Register name</th>
<th>Type</th>
<th>Description</th>
<th>CMU</th>
<th>Default (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3400</td>
<td>[0]</td>
<td>I2C_ID_SEL</td>
<td>RW</td>
<td>[0] : I2C ID Selection 0 : Vendor defined. 1 : User defined.</td>
<td>-</td>
<td>0x00</td>
</tr>
<tr>
<td>0x3401</td>
<td>[6:0]</td>
<td>I2C_ID_REG</td>
<td>RW</td>
<td>[6:0] : User defined I2C ID</td>
<td>-</td>
<td>0x30</td>
</tr>
</tbody>
</table>
10. Electrical Specification

10.1 Absolute maximum ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient storage temperature</td>
<td>$T_{ST}$</td>
<td>-30 - 85</td>
<td>°C</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>$T_{OP}$</td>
<td>-20 - 85</td>
<td>°C</td>
</tr>
<tr>
<td>Stable image temperature(1)</td>
<td>$T_{SI}$</td>
<td>0 - 60</td>
<td>°C</td>
</tr>
<tr>
<td>Analog supply voltage</td>
<td>$V_{DD-A,MAX}$</td>
<td>-0.3 - 4.0</td>
<td>V</td>
</tr>
<tr>
<td>Digital supply voltage</td>
<td>$V_{DD-D,MAX}$</td>
<td>-0.3 - 2.0</td>
<td>V</td>
</tr>
<tr>
<td>IO supply voltage</td>
<td>$V_{DD-IO,MAX}$</td>
<td>-0.3 - 4.0</td>
<td>V</td>
</tr>
<tr>
<td>DC input voltage</td>
<td>$DCIN$</td>
<td>-0.3 $V_{DD-IO}+0.3$</td>
<td>V</td>
</tr>
<tr>
<td>ESD rating</td>
<td>Human Body Model</td>
<td>- 2000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Machine Model</td>
<td>- 200</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note:**
1. The sensor will produce stable images within the temperature range and the operating limits of the electrical specification. The image quality is not guaranteed when operating the sensor beyond the stable image temperature specification.
2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 10.1: Absolute maximum ratings

10.2 Operating voltages

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog supply voltage</td>
<td>$V_{DD-A}$</td>
<td>2.6 - 2.8</td>
<td>V</td>
</tr>
<tr>
<td>Digital supply voltage</td>
<td>$V_{DD-D}$</td>
<td>1.35 - 1.65</td>
<td>V</td>
</tr>
<tr>
<td>LDO supply voltage</td>
<td>$V_{DD-LDOIN}$</td>
<td>1.7 - 3.0</td>
<td>V</td>
</tr>
<tr>
<td>IO supply voltage</td>
<td>$V_{DD-IO}$</td>
<td>1.7 - 3.0</td>
<td>V</td>
</tr>
</tbody>
</table>

Table 10.2: Operating voltages
10.3 DC characteristics

The power consumptions are measured in sense \((C_L = 5\text{pF})\).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{DD-AVDD}</td>
<td>Active current</td>
<td>External Internal LDO Mode, 8-bit RAW, QVGA @ 60fps, PCLKO gated, (V_{DD-A} = 2.8\text{V}, V_{DD-D} = 1.5\text{V}, V_{DD-IO} = 1.8\text{V})</td>
<td>-</td>
<td>271</td>
</tr>
<tr>
<td>I_{DD-DVDD}</td>
<td>Active current</td>
<td>Internal LDO Mode, 8-bit RAW, QVGA @ 60fps, PCLKO gated, (V_{DD-A} = 2.8\text{V}, V_{DD-D} = 2.8\text{V})</td>
<td>-</td>
<td>1201</td>
</tr>
<tr>
<td>I_{DD-IIOVDD}</td>
<td>Standby</td>
<td>External Internal LDO Mode, (V_{DD-A} = 2.8\text{V}, V_{DD-D} = 1.5\text{V}, V_{DD-IO} = 1.8)</td>
<td>-</td>
<td>105.7</td>
</tr>
<tr>
<td>DD-STAND BY</td>
<td></td>
<td>Internal LDO Mode, (V_{DD-A} = 2.8\text{V}, V_{DD-D} = 2.8\text{V})</td>
<td>-</td>
<td>142.3</td>
</tr>
</tbody>
</table>

**Digital Inputs (MCLK, TRIG, SCL)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IL}</td>
<td>Input Voltage Low</td>
<td>GND - 0.3</td>
<td>-</td>
<td>0.3V_{DD-IO}</td>
</tr>
<tr>
<td>V_{IH}</td>
<td>Input Voltage High</td>
<td>0.7V_{DD-IO}</td>
<td>-</td>
<td>V_{DD-IO} + 0.3</td>
</tr>
<tr>
<td>C_{IN}</td>
<td>Input Capacitance</td>
<td>-</td>
<td>4</td>
<td>pF</td>
</tr>
</tbody>
</table>

**Digital Output**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{OL}</td>
<td>Output Voltage Low</td>
<td>-</td>
<td>-</td>
<td>0.2V_{DD-IO}</td>
</tr>
<tr>
<td>V_{OH}</td>
<td>Output Voltage High</td>
<td>0.8V_{DD-IO}</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>C_{OUT}</td>
<td>Output Capacitance</td>
<td>-</td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td>R_{OUT}</td>
<td>Output Resistance</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>IOZ</td>
<td>Tri-state Leakage Current</td>
<td>-</td>
<td>-</td>
<td>10</td>
</tr>
</tbody>
</table>

**Table 10.3: DC characteristics**

10.4 Master clock input (MCLK)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCLK</td>
<td>Input frequency</td>
<td>-</td>
<td>3</td>
<td>36</td>
</tr>
<tr>
<td>MCLK_{DUTY}</td>
<td>Input clock duty cycle</td>
<td>-</td>
<td>45</td>
<td>55</td>
</tr>
</tbody>
</table>

**Table 10.4: Master Clock (MCLK) timing**
10.5 Serial bus characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F_{SCL}</td>
<td>Input clock frequency</td>
<td>-</td>
<td>100</td>
<td>400</td>
</tr>
<tr>
<td>t_{SCL}</td>
<td>Input clock period</td>
<td>-</td>
<td>2.5</td>
<td>10</td>
</tr>
<tr>
<td>-</td>
<td>Input clock duty cycle</td>
<td>-</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>t_{RT}</td>
<td>Rise time of SCL/SDA</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_{FT}</td>
<td>Fall time of SCL/SDA</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>t_{HD_SU}</td>
<td>Start setup time</td>
<td>Write</td>
<td>T_{MCLK}</td>
<td>-</td>
</tr>
<tr>
<td>t_{HD_STA}</td>
<td>Start hold time</td>
<td>Write</td>
<td>3T_{MCLK}</td>
<td>-</td>
</tr>
<tr>
<td>t_{HD_DAT}</td>
<td>Data hold time</td>
<td>Write</td>
<td>5</td>
<td>-</td>
</tr>
<tr>
<td>t_{SU_DAT}</td>
<td>Data setup time</td>
<td>Write</td>
<td>3T_{MCLK}</td>
<td>-</td>
</tr>
<tr>
<td>t_{HD_STP}</td>
<td>Stop setup time</td>
<td>Write</td>
<td>3T_{MCLK}</td>
<td>-</td>
</tr>
<tr>
<td>t_{HD_DATR}</td>
<td>Data hold time</td>
<td>Read</td>
<td>3T_{MCLK}</td>
<td>-</td>
</tr>
<tr>
<td>t_{SU_DATR}</td>
<td>Data setup time</td>
<td>Read</td>
<td>T_{SCL}/2-</td>
<td>-</td>
</tr>
<tr>
<td>C_{SDA_LOAD}</td>
<td>SDA maximum load</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>R_{SDA}</td>
<td>SDA pull-up resistor</td>
<td>-</td>
<td>500</td>
<td>-</td>
</tr>
</tbody>
</table>

Note: (1) T_{MCLK} = Cycle time of MCLK, T_{SCL} = Cycle time of SCL.

### Table 10.5: Serial bus interface timing

![Serial bus interface timing diagram](image-url)

Figure 10.1: 2-wire serial interface timing diagram
10.6 Parallel interface timing characteristics

Conditions: $T_A = 25^\circ C$, $C_L = 5pF$, $F_{PCLKO} = 12MHz$

![Parallel Interface Timing Diagram](image)

Figure 10.2: 4-bit parallel video interface timing diagram

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{PLOKO}$</td>
<td>PCLKO period</td>
<td>-</td>
<td>83.29</td>
</tr>
<tr>
<td>$T_{PR}$</td>
<td>PCLKO rise time</td>
<td>-</td>
<td>14.35</td>
</tr>
<tr>
<td>$T_{PF}$</td>
<td>PCLKO fall time</td>
<td>-</td>
<td>10.53</td>
</tr>
<tr>
<td>$T_D$</td>
<td>PCLKO falling edge to HSYNC, VSYNC rising edge delay</td>
<td>-</td>
<td>69.6</td>
</tr>
<tr>
<td>$T_{DD}$</td>
<td>PCLKO falling edge to DATA transition delay</td>
<td>-</td>
<td>88</td>
</tr>
<tr>
<td>$T_{SU}$</td>
<td>Data bus setup time</td>
<td>-</td>
<td>37.2</td>
</tr>
<tr>
<td>$T_{HD}$</td>
<td>Data bus hold time</td>
<td>-</td>
<td>43.6</td>
</tr>
</tbody>
</table>

Table 10.6: 4-bit parallel video interface timing
10.7 Serial interface timing characteristics

Conditions: \( T_A = 25^\circ C, C_L = 5\, \text{pF}, F_{\text{PLCKO}} = 36\, \text{MHz} \)

![Serial video interface timing diagram](image)

**Figure 10.3: Serial video interface timing diagram**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Name</th>
<th>Spec.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{\text{PLCKO}} )</td>
<td>PCLKO period</td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>27.78</td>
</tr>
<tr>
<td>( T_{\text{PRT}} )</td>
<td>PCLKO rise time</td>
<td></td>
<td>6.19</td>
</tr>
<tr>
<td>( T_{\text{PFT}} )</td>
<td>PCLKO fall time</td>
<td></td>
<td>5.72</td>
</tr>
<tr>
<td>( T_D )</td>
<td>PCLKO falling edge to HSYNC, VSYNC rising edge delay</td>
<td></td>
<td>23.4</td>
</tr>
<tr>
<td>( T_{\text{OD}} )</td>
<td>PCLKO falling edge to DATA transition delay</td>
<td></td>
<td>31.2</td>
</tr>
<tr>
<td>( T_{\text{SU}} )</td>
<td>Data bus setup time</td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>11.5</td>
</tr>
<tr>
<td>( T_{\text{HD}} )</td>
<td>Data bus hold time</td>
<td></td>
<td>15.2</td>
</tr>
</tbody>
</table>

**Table 10.7: Serial video interface timing**
11. Chief Ray Angle

![Figure 11.1: Chief ray angle](image)

<table>
<thead>
<tr>
<th>Field (%)</th>
<th>Image Height (mm)</th>
<th>CRA (degree)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>0</td>
<td>0.00</td>
</tr>
<tr>
<td>0.10</td>
<td>0.08</td>
<td>2.87</td>
</tr>
<tr>
<td>0.20</td>
<td>0.16</td>
<td>5.77</td>
</tr>
<tr>
<td>0.30</td>
<td>0.24</td>
<td>8.74</td>
</tr>
<tr>
<td>0.40</td>
<td>0.32</td>
<td>11.75</td>
</tr>
<tr>
<td>0.50</td>
<td>0.4</td>
<td>14.80</td>
</tr>
<tr>
<td>0.60</td>
<td>0.48</td>
<td>17.86</td>
</tr>
<tr>
<td>0.70</td>
<td>0.56</td>
<td>20.93</td>
</tr>
<tr>
<td>0.80</td>
<td>0.64</td>
<td>23.99</td>
</tr>
<tr>
<td>0.90</td>
<td>0.72</td>
<td>27.04</td>
</tr>
<tr>
<td>1.00</td>
<td>0.8</td>
<td>30.05</td>
</tr>
</tbody>
</table>

Table 11.1: Chief ray angle